Remarks/Arguments:

The present invention relates to a charge coupled device (CCD) imaging apparatus that has a drive pulse switching circuit. The switching circuit generates CCD read pulses periodically at a first frame rate and generates a CCD drive pulse at a second frame rate. The second frame rate is n/2 times the first frame rate, where n is an integer greater than 2. The CCD imaging apparatus also includes a CCd operable in a progressive scanning mode. The CCD captures an image responsive to the CCD read pulses. The CCD imaging apparatus also includes a CCD driver for driving the CCD with the CCD drive pulse to allow the CCD to output a signal corresponding to the captured image. The CCD imaging apparatus further includes a frame memory. The frame memory stores a signal of the signal output from the CCD corresponding to one frame after each of the CCD read pulses. The frame memory also reads out the stored signal n/2 times.By this Amendment, Applicants have amended claim 1. Claims 5-7 and 15-24 have been withdrawn from consideration. Claims 1-24 are pending.

Figures 2, 5, 9, 10 and 16 were objected to. Various blocks have been labeled in accordance with the Examiner's suggestion. Withdrawal of the objection is respectfully requested.

Figures 19 and 20 were objected to for not being designated as "PRIOR ART." The figures have been appropriately amended. Withdrawal of the objection is respectfully requested.

The title of the invention was objected to. The title has been amended.

Claims 1-4 and 8-13 were rejected under 35 U.S.C § 103(a) as being unpatentable over Applicant's Admitted Prior Art (AAPA) in view of Schmale. It is respectfully submitted, however, that the claims are now patentable over the art of record for the reasons set forth below.

AAPA discloses a CCD imaging device including a drive pulse generator 53 which generates a drive pulse corresponding to a mode according to a mode switching signal and sends the pulse to a CCD driver 52. (Specification at page 2, lines 20-24). As shown in Figure 20, a CCD drive pulse may be generated at n/2 times the first frame rate. For example, when a 60i mode is selected, a drive pulse shown in Fig. 20B is generated. In this case of the interlace scanning, a CCD read pulse is issued in every 1/60 second.

Applicants' invention, as recited by claim 1, includes a feature which is neither disclosed nor suggested by the art of record, namely:

> ...a drive pulse switching circuit for generating CCD read pulses periodically at a first frame rate, and for generating a CCD drive pulse at a second frame rate being n/2 times the first frame rate, n **being an integer greater than 2.** (Emphasis added).

Thus, a drive pulse switching circuit is capable of generating CCD drive pulse at a second frame rate n/2 times the first frame rate, where **n is an integer greater than 2.** (Emphasis added). This feature is found in the originally filed application at page 9, lines 8-15 and Figures 3 and 4. No new matter has been added.

AAPA does not disclose or suggest a drive pulse switching circuit capable of generating CCD drive pulse at a second frame rate n/2 times the first frame rate, where n is an integer greater than 2. Thus, Applicants' drive pulse generator 9 can generate a multiplied CCD drive pulse greater than the drive pulse. For example, the drive pulse generator may generate in the 25p mode. Next, the (n/2) multiplier 14 may, for example, generate a double-rate CCD drive pulse, such as a 50p mode drive pulse in the case of n=4, respectively. (Specification at page 9, lines 1-14).

This feature has the advantage of displaying an image without flicker. In the 25p mode example stated above, the VF 6 displays an image at a frame rate of the 50p mode. The VCR unit 7 records an image at the 50p frame rate as a 25p signal by adjusting the recording speed.

Thus, when a preset frame rate is, in this example, 50 frames/sec or less, the VF displays an image at a frame rate of (n/2) times of the preset rate (where n is an integer), for example, at a double of the preset rate. Therefore, the VF displays the image without flicker. Further, the CCD signal is vertically transferred in a short time, and thus prevents a performance of the CCD from deterioration.

Schmale discloses a camera including a memory circuit 8 which stores the output of a CCD 2 prior to reading out the stored signal and sending it to a signal processing circuit 3. The memory circuit allows a user to freeze a scene and make adjustments to the signal processing circuit without requiring the scene to be motionless.

Applicants' invention, as recited by claim 1 includes a feature which is neither disclosed nor suggested by the art of record, namely:

> ...a frame memory for storing a signal of the signal output from said CCD corresponding to one frame **after each of the CCD read pulses**, and for reading out the stored signal **n/2 times**. (Emphasis added).

Thus, a frame memory is for storing a signal of the signal output from the CCD corresponding to one frame after each of the CCD read pulses. The frame memory also reads out the stored signal n/2 times. The CCD read pulses are generated periodically at a first frame rate. These features are found in the originally filed application at page 9, lines 22-26 and page11, line 26 to page 12 line 3. No new matter has been added.

Schmale does not disclose or suggest a frame memory for storing a signal of the signal output from the CCD corresponding to one frame after each of the CCD read pulses and a frame memory which reads out the stored signal n/2 times. The Official Action asserts that it is obvious to combine the memory device in Schmale with the CCD imaging apparatus "to allow a user to freeze a scene and make adjustments to the signal apparatus without requiring the scene to be motionless."

Applicants' claimed frame memory stores a signal of the signal output from the CCD corresponding to one frame **after each of the CCD read** pulses. (Emphasis added). The frame memory also reads out the stored signal **n/2 times**. The n/2 multiplier, which may generate a drive pulse at a greater rate than the first rate allows the present invention to adjust to parameters without stopping. (Emphasis added). Thus, the present application does not have to stop or freeze an image to make adjustments and does not require the image to be motionless at any time.

Schmale requires the image output from a frame memory to be motionless. Schmale attempts to adjust a video signal in accordance with adjustment parameters by freezing the input image. Thus, Schmale must stop or freeze the image to make adjustments. It is because Applicants claim the feature of multiplying the first frame rate - "generating ... a second frame rate being n/2 the first frame rate" - that adjustments can be made without stopping and without requiring the image to be motionless at any time.

Neither AAPA, Schmale nor their combination disclose or suggest a drive pulse switching circuit capable of generating CCD drive pulse at a second frame rate n/2 times the first frame rate, where n is an integer greater than 2. Further, neither AAPA, Schmale nor their combination disclose or suggest a frame memory for storing a signal of the signal output from the CCD corresponding to one frame after each of the CCD read pulses and then reads out the stored signal n/2 times.

Accordingly, for the reasons set forth above, claim 1 is patentable over the art of record.

Claims 2-3 and 8-12 include all the features of claim 1 from which they depend. Thus, claims 2-3 and 8-12 are also patentable over the art of record for the reasons set forth above.

In view of the amendments set forth above, the above-identified application is in condition for allowance which action is respectfully requested.

Respectfully submitted,

Lawrence E. Ashery, Reg. No. 34,515
Attorney for Applicants

DDF/fp/ddf/ds

Attachments: Figures 2, 5, 9, 10, 16, 19 and 20 (7 sheets)

Dated: August 19, 2005

P.O. Box 980
Valley Forge, PA 19482-0980
(610) 407-0700

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Deborah Spratt Deborah Spratt

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Amendments to the Drawings:

The attached sheets of drawings include changes to Figures 2, 5, 9, 10, 16, 19 and 20. These sheets replace the original sheets.